SYSTEM AND METHOD FOR THE DIRECTIONAL RECEPTION AND DESPREADING OF DIRECT-SEQUENCE SPREAD-SPECTRUM SIGNALS

invented by

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TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates to the field of spread-spectrum receivers. More specifically, the present invention relates to the field of direct-sequence spread-spectrum receivers and despreaders.

BACKGROUND OF THE INVENTION

[0002] Direct-sequence spread-spectrum (DSSS) radio signals are used in many applications. One such application is the Global Positioning System (GPS), which provides timing and positioning data for use worldwide. The GPS uses code-division multiple-access (CDMA) signals (i.e., DSSS signals) which are broadcast from a constellation of twenty-four MEO (medium Earth orbit) satellites at approximately 20,100 km altitude. By being so located, these satellites may provide GPS signals to low Earth orbit (LEO) and terrestrial receivers.

[0003] The encoding used in such CDMA signals may be any of several types. For example, standardized C-code, P/Y code and future M-code systems are of interest.

[0004] The receivers for conventional military GPS signals desirably use beam forming to minimize interference and/or jamming. Commercial applications of beam forming reduce undesirable multipath effects. Beam forming is conventionally performed through the use of analog circuitry in the time domain. This analog circuitry requires the use of precision components and careful thermal tracking. This results in a significant manufacturing cost in both monies and time as well as a cumbersome circuit card mass.

[0005] The despreading of DSSS signals conventionally requires complex correlation. With M-code GPS receivers, despread synchronization often requires a significant time.

Desirably, such receivers use multiple parallel despreaders for rapid synchronization of the M-code. This results in a significant increase in circuit complexity.

[0006] Analog beam formers and multiple parallel correlators result in a circuit that is large, complex, and potentially fragile. This results in a significant increase in costs for a number of reasons: circuit "real estate" (i.e., size), circuit power consumption, and circuit reliability.

[0007] In addition, CDMA GPS and other DSSS signals are susceptible to jamming and other narrowband interference. This interference may render the desired signal totally unusable to the receiver.

SUMMARY OF THE INVENTION

[0008] Accordingly, it is an advantage of the present invention that a system and method for the reception and despreading of direct-sequence spread-spectrum (DSSS) signals are provided.

[0009] It is another advantage of the present invention that a system and method of simplified beam formation and despreading are effected without a need for a plurality of parallel beam formers and/or despreaders.

[0010] It is another advantage of the present invention that a system and method of simplified beam formation are provided that effect beam formation in the frequency domain.

[0011] It is another advantage of the present invention that the simplified method of beam formation provides the ability to reduce narrowband interference or jamming by filtering the beam formed.

[0012] It is another advantage of the present invention that a system and method of simplified despreading of the DSSS signal are provided that effect despreading in the frequency domain.

[0013] The above and other advantages of the present invention are carried out in one form by a system for the reception and despreading of a DSSS signal, where the system includes an antenna array having a plurality of elements to receive the signal, a preprocessor to preprocess the signal in the time domain, a first transformer to transform the DSSS signal into the frequency domain, a beam former to form a reception beam in the signal in the frequency domain, a despreader to despread the signal in the frequency domain, and a second transformer to transform the despread signal back into the time domain.

[0014] The above and other advantages of the present invention are carried out in another form by a method of receiving a direct-sequence spread-spectrum signal, where the method includes receiving the signal at each of a plurality of antenna elements in an antenna array, preprocessing the signal in the time domain, transforming the signal into the frequency domain, forming a reception beam for the signal in the frequency domain, despreading the signal in the frequency domain, and transforming the signal back to the time domain.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] A more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the Figures, wherein like reference numbers refer to similar items throughout the Figures, and:

[0016] FIG. 1 shows a schematic block diagram depicting overall operation of a system for the reception and despreading of a direct-sequence spread-spectrum (DSSS) signal in accordance with a preferred embodiment of the present invention.

[0017] FIG. 2 shows a schematic block diagram depicting operation of a preprocessor for the system of FIG. 1 in accordance with a preferred embodiment of the present invention;

[0018] FIG. 3 shows a schematic block diagram depicting operation of a beam-former and despreader for the system of FIG. 1 in accordance with a preferred embodiment of the present invention;

[0019] FIG. 4 shows a schematic block diagram depicting detailed operation of the beam former and despreader of FIG. 3 in accordance with a preferred embodiment of the present invention; and

[0020] FIG. 5 shows a schematic block diagram depicting operation of a postprocessor for the system of FIG. 1 in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] To minimize confusion, physical components are assigned reference numbers in the 100s, while signals, reception beams, signal streams and segments thereof, clocks, data codes, and the like are assigned reference numbers in the 200s.

[0022] FIG. 1 shows a schematic block diagram depicting the overall operation of a system 100 for the reception and despreading of a wideband direct-sequence spread-spectrum (DSSS) signal 200 in accordance with a preferred embodiment of the present invention. System 100 is configured to receive, form reception beams 201 in, and despread DSSS signal 200. In the context of this discussion, reception beam 201 is a received-signal analog of a transmission beam were system 100 a transmission system. In other words, reception beam 201 provides reception directionality for antenna array 102 in the reception of DSSS signal 200.

[0023] In the preferred embodiment, DSSS signal is a code-division multiple-access (CDMA) signal, specifically a global positioning system (GPS) signal. Those skilled in the art will appreciate, however, that system 100 may readily be adapted to DSSS signals other than a CDMA GPS signal, including, but not limited to, conventional CDMA cellular radio telephony and other

forms of communication, without departing from the spirit of the present invention.

[0024] DSSS signal 200 is received by an antenna array 102 and passed to a preprocessor 104. Preprocessor 104 preprocesses (i.e., processes prior to beam forming and despreading) DSSS signal 200 into a time-domain (TD) DSSS signal stream 202. The operation of preprocessor 104 is discussed in more detail hereinafter in conjunction with FIG. 2.

[0025] TD DSSS signal stream 202 then passes to a transformer 106. In transformer 106, TD DSSS signal stream 202 is transformed from the time domain to the frequency domain to produce a frequency-domain (FD) TDSS signal stream 204. Transformer 106 is a time-to-frequency domain (TFD) transformer 106. In the preferred embodiment, TFD transformer 106 performs a fast-Fourier transform (FFT). Those skilled in the art will appreciate that transforms other than an FFT may be used to transform TD DSSS signal stream 204 from the time domain to the frequency domain without departing from the spirit of the present invention. The operation of TFD transformer 106 is discussed in more detail hereinafter in conjunction with FIGs. 3 and 4.

[0026] FD DSSS signal stream 204 then passes to a beam former 108. Beam former 108 forms a plurality of beamed signal streams 206 in the frequency domain. The formation of beamed signal streams 206 effects the formation of reception beams 201 for the original DSSS signal 200. In the context of this discussion, reception beam 201 is a received-signal analog of a transmission beam were system 100 a transmission system. In other words, reception beam 201 provides reception directionality for antenna array 102 in the reception of DSSS signal 200. The operation of beam former 108 is discussed in more detail hereinafter in conjunction with FIGs. 3 and 4.

[0027] Beamed signal streams 206 are then passed to a despreader 110. Despreader 110 despreads beamed signal streams 206 into an FD despread signal stream 208 in the frequency

domain. The operation of despreader 110 is discussed in more detail hereinafter in conjunction with FIGs. 3 and 4.

[0028] FD despread signal stream 208 then passes to a transformer 112. Transformer 112 transforms FD despread signal streams 208 from the frequency domain to the time domain to produce a TD despread signal stream 210. Transformer 112 is therefore a frequency-to-time domain (FTD) transformer 112. In the preferred embodiment, FTD transformer 112 is an inverse fast-Fourier transformer (IFFT). Those skilled in the art will appreciate that transformers other than an IFFT may be used to transform FD despread signal streams 208 from the frequency domain to the time domain without departing from the spirit of the present invention. The operation of FTD transformer 112 is discussed in more detail hereinafter in conjunction with FIGs. 3 and 4.

[0029] FD despread signal stream 210 then passes to a postprocessor 114. Postprocessor 114 postprocesses FD despread signal stream 210 to produce a received signal stream 212. Postprocessor 114 is discussed hereinafter in more detail in conjunction with FIG. 5.

[0030] FIG. 2 shows a schematic block diagram depicting the operation of antenna array 102 and preprocessor 104 of system 100 in accordance with a preferred embodiment of the present invention. The following discussion refers to FIGs. 1 and 2.

[0031] DSSS signal 200 is received by antenna array 102. Antenna array 102 is made up of a plurality of antenna elements 116. At each antenna element 116, DSSS signal 200 is received as a DSSS elemental signal 214, i.e., as the signal received at that one antenna element 116.

[0032] Each DSSS elemental signal 214 then enters preprocessor 104, where it passes into one of a plurality of digitizers 118. There is a one-to-one relationship between antenna elements 116 and digitizers 118. Each digitizer 118 down

converts, and digitizes DSSS elemental signal 214 to produce a DSSS baseband signal 216.

[0033] Within each digitizer 118, DSSS elemental signal 214 passes into an analog down converter 120, where DSSS elemental signal 214 is down converted using conventional techniques to produce a DSSS converted signal 218. DSSS converted signal 218 is, in effect, an intermediate-frequency signal. Those skilled in the art will appreciate that, in some applications, analog down converter 120 may be omitted without departing from the spirit of the present invention. If analog down converter 120 were to be omitted, DSSS converted signal 218 would be DSSS elemental signal 214.

[0034] DSSS converted signal 218 then passes into an analog-to-digital (A/D) converter 122. A/D converter 122 digitizes DSSS converted signal 218 to produce a DSSS digitized signal 220.

[0035] DSSS digitized signal then passes into a digital down converter 124. Digital down converter 124 down converts DSSS digitized signal 220 into a near baseband signal 216 having only unknown frequency error and Doppler shift. Since DSSS digitized signal 220 is a digital signal, digital down converter 124 may be realized as a simple multiplier, though this is not a requirement of the present invention.

[0036] With DSSS baseband signals 216, DSSS elemental signals 214 have been down converted and digitized. DSSS baseband signals 216 are the outputs of digitizers 118.

[0037] Those skilled in the art will appreciate that digitizers 118, and the components therein (i.e., analog down converters 120, A/D converters 122, and digital down converters 124) are exemplary of the preferred embodiment only. Other techniques and circuitry may be used to produce DSSS baseband signals 216 without departing from the spirit of the present invention.

[0038] DSSS signal 200 is received at each antenna element 116. However, due to the spacing between antenna elements 116, each DSSS elemental signal 214 has a potentially unique phase depending upon the direction from which a transmitted DSSS signal 200 originates. All digitizers 118 are substantially identical. The phase relationships between DSSS elemental signals 214 are therefore maintained in DSSS baseband signals 216. Each DSSS baseband signal 216 potentially differs from each other DSSS baseband signal 216 solely in phase.

[0039] From each digitizer 118, DSSS broadband signal 216 passes to a presummer 126. Presummer 126 adjusts DSSS baseband signal 216 preparatory to fracturing (discussed hereinafter). Taken together, the adjustments effected by presummers 126 result in each DSSS baseband signal 216 being segmented and displaced in time a predetermined amount while preserving the phase relationships between DSSS baseband signals 216. As is well known in the art, the degree of presumming performed by presummer 126 is relevant to the signal bandwidth. The output of each presummer 126 is DSSS adjusted signal 222.

[0040] Each DSSS adjusted signal 222 passes into a multi-access memory 128. Multi-access memory 128 fractures DSSS adjusted signal 222 into a plurality of DSSS signal-stream segments 224. Each DSSS signal-stream segment 224 is a portion of DSSS adjusted signal 222 (as segmented and displaced by presummer 126).

[0041] In this discussion, the term "multi-access memory" may be taken to mean any circuit that performs the function of a multi-access memory. In the preferred embodiment, each multi-access memory 128 is a cluster of three ping-pong random-access memories (PP RAM) 130 which cycle DSSS signal-stream segments 224 preparatory to multiplexing (discussed hereinafter). In other embodiments, multi-access memory 128 may be conventional random-access memory (RAM) where the multi-access aspect is performed though any of numerous well-known addressing schemes.

[0042] Alternatively, multi-access memory 128 may be implemented though the use of shift registers and other well-known techniques. Those skilled in the art will appreciate that the specific methodology used to implement multi-access memories 128 is not a requirement of the present invention. The use of a specific methodology does not depart from the spirit of the present invention.

[0043] In the preferred embodiment, each multi-access memory 128 stores each segment of DSSS adjusted signal 222 in a sequentially rotary manner. Starting at an arbitrary time, a first segment is stored in a first PP RAM 130, a second segment in a second PP RAM 130, a third segment in a third PP RAM 130, a fourth segment in the first PP RAM 130, and so on. Multi-access memories 128 associated with each antenna element 116 perform these storages in parallel. This results in temporally identical segments of each DSSS adjusted signal 222 being stored in the corresponding PP RAM 130 in each multi-access memory 128 (e.g., in the first PP RAM 130 of each multi-access memory).

[0044] DSSS signal-stream segments 224 from each multi-access memory 128 then pass into a multiplexer 132. Multiplexer 132 cyclically multiplexes temporally identical DSSS signal-stream segments 224 from each multi-access memory 128 to produce TD DSSS signal stream 202 in the time domain. Due to the synchronization and displacement provided DSSS adjusted signals 216 by presummers 126, TD DSSS signal stream 202 is made up of consecutive segments, e.g., (assuming four antenna elements 116 "A," "B," "C," and "D") a first "A" segment (derived from element "A"), a first "B" segment (derived from element "B"), a first "C" segment (derived from element "C"), a first "D" segment (derived from element "D"), a second "A" segment, a second "B" segment, a second "C" segment, a second "D" segment, a third "A" segment, a third "B" segment, etc. TD DSSS signal stream 202 is therefore a stream of serially interleaved DSSS signal-stream segments 224 forming a composite of signal-stream segments derived from all

DSSS elemental signals 214. In the preferred embodiment, the data rate is "N" times the data rate of each DSSS adjusted signal 216, where "N" is equal to the number of antenna elements 116.

[0045] In the preferred embodiment, multiplexer 132 is a conventional physical multiplexer. Those skilled in the art will appreciate that, in many cases, multiplexing may be performed without the use of a conventional physical multiplexer. It will be appreciated, therefore, that in this context the term "multiplexer" may be taken to mean any circuit or arrangement of components that multiplexes, i.e., fulfills the function of a conventional physical multiplexer. The use of any scheme other than a conventional physical multiplexer does not depart from the spirit of the present invention.

[0046] FIGs. 3 and 4 show a schematic block diagram depicting the operation of beam-former 108 and despreader 110 for system 100 in accordance with a preferred embodiment of the present invention. FIG. 3 demonstrates a physical perspective, and FIG. 4 demonstrates a "logical" or effective perspective of the operation. TFD and FTD transformers 106 and 112 have been included in FIGs. 3 and 4 for clarity. The following discussion refers to FIGs. 1, 2, 3, and 4.

[0047] TFD transformer 106 transforms TD DSSS signal stream 202 from the time domain to the frequency domain and produces FD DSSS signal stream 204. TD DSSS signal stream 202 contains a steady stream of DSSS signal-stream segments 224 in the time domain, i.e., serially in time. Each segment, under control of presummer 126, multi-access memory 128 and multiplexer 132 (FIG. 2), represents a "block" of information (not necessarily associated with a "block of data" as transmitted in DSSS signal 200) having a predetermined size. TDF transformer 106 is sized and synchronized in harmony with multi-access memory 128 and multiplexer 132 so that TDF transformer 106 serially transforms each segment in turn. Therefore, after the transformation of TD DSSS signal stream 202 to the frequency

domain, FD DSSS signal stream 204 contains a stream of sequential signal-stream segments, where each segment has been transformed into a plurality of frequency "bins" (not shown) by TFD transformer 106. This sequential transformation eliminates the need for multiple TFD transformers 106, and allows beam former 108 and despreader 110 to sequentially process each segment in the frequency domain, with subsequent segments being processed sequentially over time (i.e., serially).

[0048] The following discussion refers to FIGs. 1, 3, and 4.

[0049] Beam former 108 forms beamed signal streams 206 from FD DSSS signal stream 204 in response to a coefficient stream 226. A coefficient generator 134 is used to generate coefficient stream 226.

[0050] Beam coefficients 228 defining the desired reception beam 201 for DSSS signal 200 are obtained. Depending upon the application, beam coefficients 228 may be determined from a search, extracted from a table, computed, or determined from DSSS signal 200. In the preferred embodiment, where DSSS signal 200 is a CDMA GPS signal, beam coefficients 228 are computed from data received in DSSS signal 200 revealing the location of the transmitter transmitting DSSS signal 200. Because of this, system 100 of the preferred embodiment forms reception beam 201 after initial reception of DSSS signal 200, then refines reception of DSSS signal 200 in response to reception beam 201.

[0051] Similarly, filter coefficients 230 for a narrowban notch filter are obtained. Depending upon the application, filter coefficients 230 may be extracted from a table, measured, or computed. In the preferred embodiment, filter coefficients 230 are computed for narrowband signals. Such narrowband signals are construed as interference or jamming (i.e., intentional interference). In the preferred embodiment, filter coefficients 230 may be computed for known narrowband interference existing

within the wideband occupied by DSSS signal 200. While not explicitly shown in the Figures nor discussed in detail herein, it will be appreciated that a search and conquer technique may be used where filter coefficients 230 are generated in real time for narrowband interference detected in real time,

[0052] Those skilled in the art will appreciate that the methodology used to obtain beam and filter coefficients 228 and 230 is not a requirement of the present invention. Alternative methodologies may be used without departing from the spirit of the present invention.

[0053] A multiplier 136 combines beam coefficients 228 and filter coefficients together to produce combined coefficients 232. Those skilled in the art will appreciate that the existence of filter coefficients 230 is dependent upon the existence of an interfering signal. Filter coefficients 230 may be eliminated (i.e., made unitary). In this case, multiplier 136 does nothing and combined coefficients 232 are substantially equal to beam coefficients 228.

[0054] A memory 138 stores and releases combined coefficients 232 to produce coefficient stream 226 to provide synchronization with FD DSSS signal stream 204.

[0055] Within beam former 108, a multiplier 140 mixes FD DSSS signal stream 204 with coefficient stream 226. This results in a plurality of partial-beam signal streams 234. FD DSSS signal stream 204 contains a serial stream of segments. Multiplier 140 processes each segment serially. In this manner, a single physical multiplier 140 (FIG. 3), by acting serially, serves the function of a plurality of virtual multipliers 140' (FIG. 4), where each virtual multiplier 140' would process the data for one frequency bin for each component of beam coefficients 228.

[0056] Also in beam former 108 is an accumulative adder 142. Accumulative adder 142 sums partial-beam signal streams 234 for a given temporally identical set of segments together to

produce a plurality of beamed signal streams 206. Since each segment is processed by multiplier 140 sequentially, accumulative adder 142 is made up of a summer 144 configured and an accumulator 146. Summer 144 sums each subsequent partial-beam signal stream 234 in turn, while accumulator 146 accumulates and passes back to summer 144 all partial sums. In this manner, one physical accumulative adder 142 serves the function of a plurality of virtual adders 142', where each virtual adder would sum all partial-beam signal streams 234 for each component of beam coefficients 228. Accumulative adder 142 therefore produces a beamed signal stream 206 for each component of beam coefficients 228.

[0057] With the formation of beamed signal streams 206, reception beams 201 for antenna array 102 come into existence. Each beam is formed in a direction determined by beam coefficients 228. In effect, signals arriving from that direction are normalized and signals arriving from other direction are attenuated.

[0058] DSSS signal 200 is a wideband signal. Within the bandwidth of DSSS signal 200, there may exist an interfering narrowband signal. Beam former 108 allows the generation of notches in the bandwidth of DSSS signal 200. These notches are at frequencies determined by filter coefficients 230. This results in severe attenuation of interfering narrowband signals at the notch frequencies.

[0059] Following beam former 208, beamed signal streams 206 pass to despreader 110. Despreader 110 despreads beamed signal streams 206 to produce FD despread signal stream 208. DSSS signal 200 is spread using a specific spread code. Beamed signal streams 206 must therefore be despread using a matching despread code. Despreader 110 therefore despreads beamed signal streams 206 in response to an FD despread-code stream 236 containing the requisite despread code.

[0060] The requisite despread codes are generated by a despread-code generator 148 in the time domain. Within despread code generator 148, a plurality of code oscillators 150 produce a plurality of code clocks 238 under control of a microprocessor (not shown). All code clocks 238 are substantially identical except for phase. A plurality of code generators 152, one for each code clock 238, then generate the requisite despread codes 240 in response to code clocks 238. The despread codes 240, also, are substantially identical except for phase. Despread codes 240 are the stored in a memory 154 and released as a TD despread-code stream 242 in the time domain. A TFD transformer 156 then transforms TD despread-code stream 242 from the time domain to the frequency domain to produce FD despread-code stream 236.

[0061] Despreader 110 despreads beamed signal streams 206 in response to FD despread code stream 236 (i.e., in response to the requisite despread codes 240). Within despreader 110, a multiplier 158 mixes each beamed signal string 206 with FD despread-code stream 236. This results in a plurality of FD despread signal streams 208. Each beamed signal stream 206 contains a serial stream of segments. Multiplier 158 processes each segment serially. In this manner, a single physical multiplier 158 (FIG. 3), by acting serially, serves the function of a plurality of virtual multipliers 158′ (FIG. 4), where each virtual multiplier 159′ would mix each beamed signal stream 206 with each despread code 240 for each component of beam coefficients 228.

[0062] Only one of the resulting FD despread signal steams 208 is viable for the signal-stream segment being processed. Beamed signal streams 206 are despread into multiple FD despread signal streams 208 in response to multiple despread codes 240 in despread-code stream 236. Since each despread code 240 has a different phase, each FD despread signal stream 208 also has a different phase. This allows for more rapid synchronization of

at least one of FD despread signal streams 208 with chip-level timing signals, being ?the desired FD despread signal stream 208. This pseudo-parallel approach allows one despreader 110 in the frequency domain to effect the operation of multiple parallel correlators (despreaders) in the time domain, and allow rapid despreading of M-code or other codes that normally would take a significant time to correlate.

[0063] FD despread signal 206 then passes to FTD transformer 112. FTD transformer 112 transforms FD despread signal 208 from the frequency domain to the time domain and produces TD despread signal stream 210.

[0064] FIG. 5 shows a schematic block diagram depicting the operation of postprocessor 114 for system 100 in accordance with a preferred embodiment of the present invention. The following discussion refers to FIGs. 1 and 5.

[0065] TD despread signal stream 210 then passes into postprocessor 114. Postprocessor 114 postprocesses (i.e., processes after beam forming and despreading) TD despread signal stream 210 to produce received signal stream 212.

[0066] Within postprocessor 114, TD despread signal stream 210 passes into a Doppler compensator 160. Within Doppler compensator 160, a plurality of carrier oscillators 162 produce a plurality of Doppler clocks 244 under control of the microprocessor (not shown). All Doppler clocks 244 are substantially identical except for phase. A multiplexer 164 then multiplexes Doppler clocks 244 to produce a Doppler compensation stream 246. A multiplier 166 then mixes TD despread signal stream 210 with doppler compensation stream 246 to produce compensated signal stream 248.

[0067] Those skilled in the art will appreciate that methodology used in Doppler compensator 160 is exemplary of the preferred embodiment only. Other methodologies, including but not limited to the exclusion of Doppler compensator 160, may be used without departing from the spirit of the present invention.

[0068] Following Doppler compensator 160, compensated signal stream 160 pass into an integrator 168. Integrator 168 effects integration of compensated signal stream 248 to produce received signal stream 212. Received signal stream 212 then passes to the microprocessor (not shown).

[0069] Those skilled in the art will appreciate that integrator 168 is exemplary of the preferred embodiment and is not a requirement of the present invention. Integrator 168 is depicted in FIG. 5 as an accumulative adder. This, too, is exemplary only and is not a requirement of the present invention. It will be appreciated that other implementations of or the omission of integrator 168 does not depart from the spirit of the present invention.

[0070] In summary, the present invention teaches a system 100 and associated method for the reception and despreading of a direct-sequence spread-spectrum (DSSS) signal 200. DSSS signal 200 is preprocessed and fractured to produce a time-domain (TD) DSSS signal stream 202. TD DSSS signal stream 202 is then transformed to the frequency domain to produce a frequency-domain (FD) signal stream 204. Reception beams 201 are formed in the frequency domain to produce a beamed signal stream 206. Beamed signal stream 206 is then despread in the frequency domain to produce an FD despread signal stream 208. FD DSSS signal stream is the transformed from the frequency domain to the time domain to produce a TD despread signal stream 210. TD despread stream 210 is then postprocessed to produce a final received signal stream.

[0071] By fracturing the signal stream and effecting beam forming and despreading in the frequency domain, operation may be performed serially with simple digital circuitry that would otherwise require parallel performance with more complex high precision analog circuitry. This results in a significant decrease in circuit complexity and fragility over the prior art. System 100 utilizes a simpler, more robust circuit exhibiting a

significant reduction in both chip real estate and power consumption over prior art systems. Although the preferred embodiments of the invention have been illustrated and described in detail, it will be readily apparent to those skilled in the art that various modifications may be made therein without departing from the spirit of the invention or from the scope of the appended claims.